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DATA SHEET

TEA1566
GreenChip™; SMPS module

Preliminary specification
File under Integrated Circuits, IC11

1999 Apr 20

Philips
Semiconductors

PHILIPS

GreenChip™; SMPS module TEA1566

FEATURES

Distinctive features

- High level of integration results in 20 to 50 fewer components compared to a power supply with discrete components
- On-chip 600 V MOSFET
- On/off function replaces expensive mains switch with functional switch
- Direct off-line operation (90 to 276 VAC)
- On-chip 5% accurate oscillator.

Green features

- Low power consumption in off-mode (<100 mW)
- On-chip efficient start-up current source giving fast start-up
- Burst mode stand-by (<2 W) for overall improved system efficiency
- Low power operation mode with lower frequency to reduce switching losses.

Protection features

- Demagnetization protection
- Cycle by cycle current limitation with programmable current trip level
- Over voltage protection
- Over temperature protection
- Safe-restart mode with reduced power for system fault conditions.

Highly versatile

- Usable in Buck and flyback topology
- Interfaces both primary and secondary side feedback.

APPLICATIONS

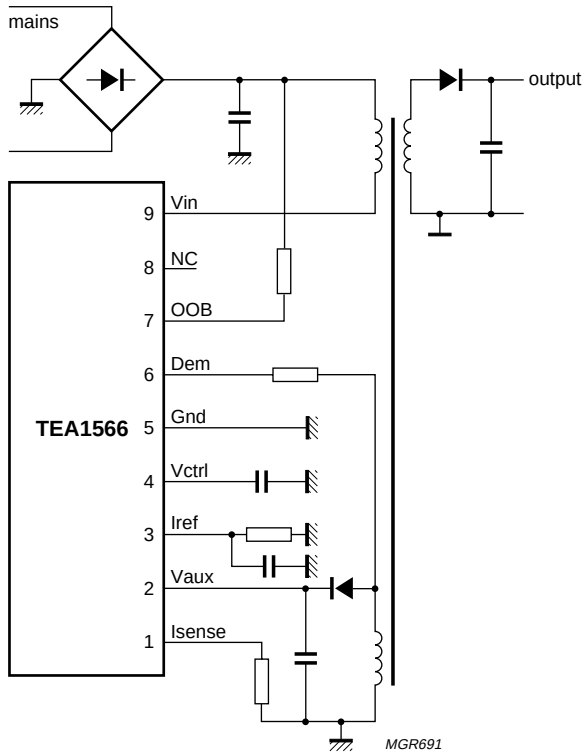


Fig.1 Typical flyback application.

GENERAL DESCRIPTION

The GreenChip™, intended for off-line 90 to 276 VAC power supply applications, is a monolithic high voltage family of ICs that combines analog and digital circuits to implement all necessary control functions for a switched mode power supply. The functions include integrated high voltage start-up current source, voltage mode PWM control, 5% accurate trimmed oscillator, band gap derived reference voltages, comprehensive fault protection, and leading edge blanking. High level of integration leads to cost effective power supplies that are compact, weigh less, and at the same time give higher efficiency, are more reliable and simple to design. Efficient green features lead to very low power operation modes and a novel on/off function helps replace the expensive mains switch with a low cost functional switch.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1566S	SIL9P	plastic single in-line power package; 9 leads	SOT131-2
TEA1566J	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length12 mm)	SOT157-2

BLOCK DIAGRAM

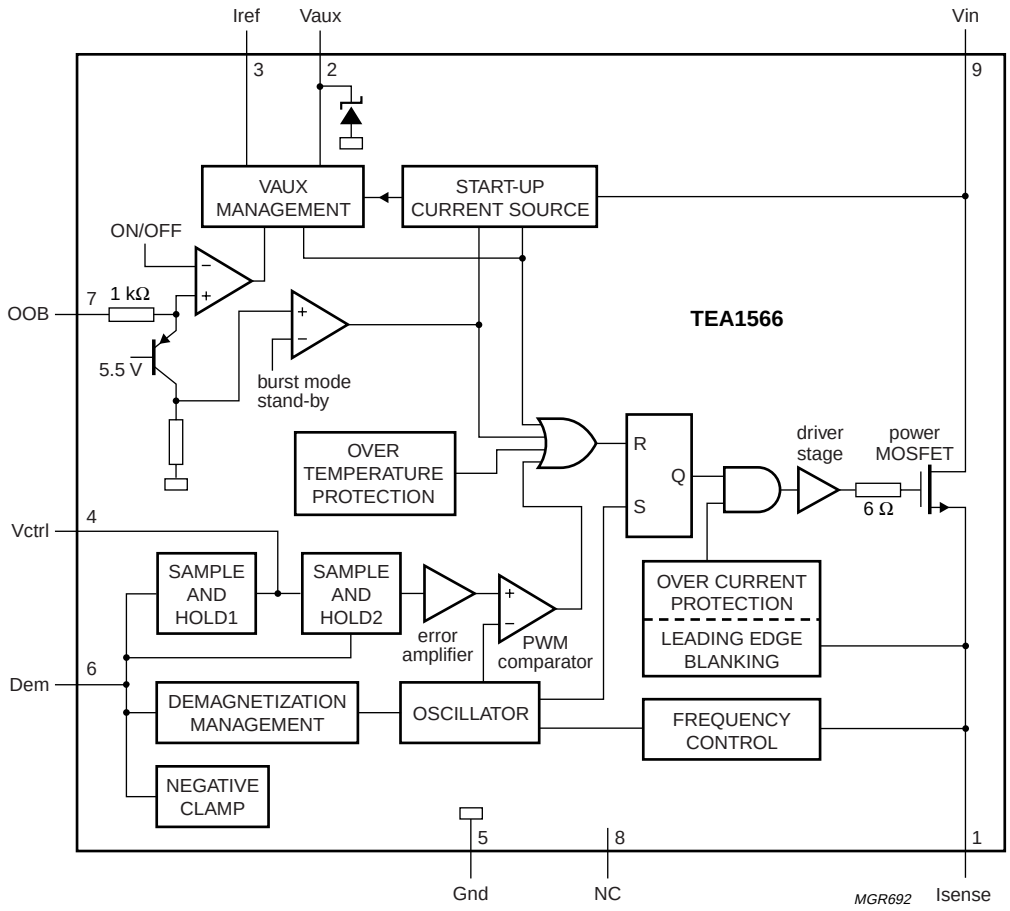


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
Isense	1	programmable current sense resistor
Vaux	2	IC supply capacitor
Iref	3	reference resistor for setting internal reference currents
Vctrl	4	feedback voltage for duty cycle control
Gnd	5	ground
Dem	6	demagnetization input signal from primary side auxiliary winding
OOB	7	on/off/burst mode input signal
NC	8	not connected
Vin	9	MOSFET drain connection

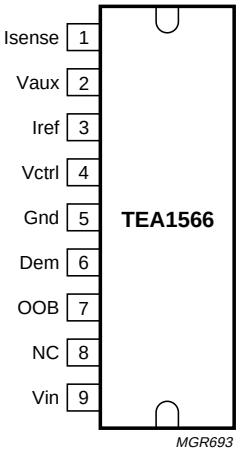


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The GreenChip™ family of ICs are highly integrated, with most common PWM functions like error amplifier, oscillator, bias current generator, and band gap based reference voltage circuits fully integrated in the ICs. High level of integration leads to easy and cost effective design of power supplies.The ICs have been fabricated in a Philips proprietary high voltage BCDMOS process that enables devices of up to 720 V to be fabricated on the same chip with low voltage circuitry.

An efficient on-chip start-up circuit enables fast start-up and dissipates negligible power after start up. On-chip accurate oscillator generates a saw tooth waveform which is used by the voltage mode feedback control circuitry to generate a pulse width modulated signal for driving the gate of the power MOSFET. A novel regulation scheme is used to implement both primary and secondary side regulation to minimize external component count. Protection features like over voltage, over current, over temperature, and demagnetization protection, give comprehensive safety against system fault conditions. The GreenChip™ offers some advanced features that greatly enhance the efficiency of the overall system. Off-mode reduces the power consumption of the IC below 100 mW. Burst mode stand-by reduces the power consumption of the system to below 2 W. Low power operation mode reduces the operating frequency of the system, when the system is working under low load conditions, to reduce the switching losses.

Start-up current source and Vaux management

A versatile on-chip start-up current source makes an external, highly dissipating, trickle-charge circuit unnecessary. See Fig.2 for the block diagram of the IC.

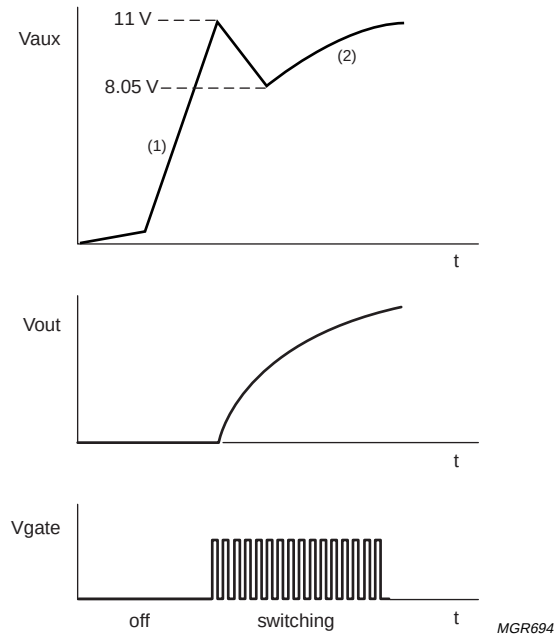
The start-up current source derives power from the mains via pin Vin (drain). It supplies current (see symbols ‘Istart-low’ and ‘Istart-high’ of Chapter “Characteristics”) to charge the Vaux (IC supply) capacitor and at the same time provides current to the control circuitry of the IC. Once the Vaux capacitor is charged to its start-up voltage level (11 V), the on-chip oscillator starts oscillating and the IC starts switching the power MOSFET. Power is then supplied to the load capacitor via the secondary winding.

Figure 1 shows a typical flyback application diagram. The Vaux capacitor is also supplied by an auxiliary winding on the primary side. This winding is coupled to the secondary side winding supplying the output capacitor. As the output capacitor voltage increases and approaches its nominal value, the re-supply of the Vaux capacitor is done by the auxiliary winding. Figure 4 shows relevant waveforms at start-up. For successful take over of supply of Vaux capacitor by the auxiliary winding, it is important that the re-supply of Vaux capacitor starts before its voltage drops to its Under Voltage Lockout (UVLO) level of 8.05 V of the system and stops delivering power to the output.

In case of output short circuit, the Vaux capacitor is no longer supplied by the auxiliary winding and its voltage drops till it reaches the UVLO level. If the output is an open circuit, the output voltage will rise till it reaches the Over Voltage Protection (OVP) level. The IC will detect this state and stop switching.

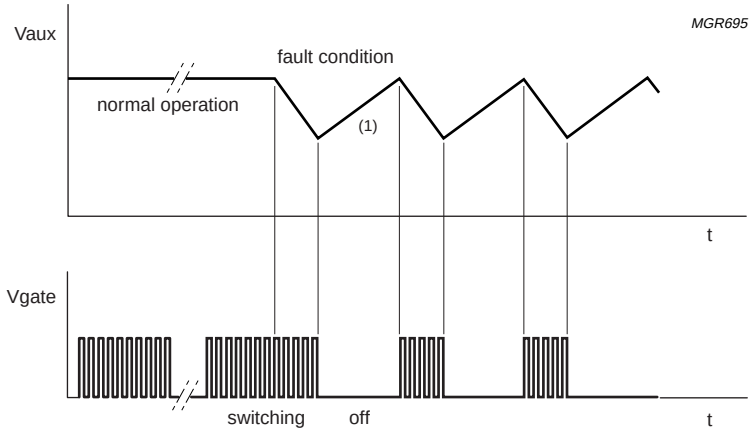
In absence of switching of the power device, the Vaux capacitor will not be re-supplied and its voltage will drop till it reaches UVLO level. Once the Vaux voltage drops to UVLO level, the start-up current source is re-activated and it charges the Vaux capacitor to its start level and the system goes through a cycle similar to the start-up cycle.

Figure 5 shows the relevant waveforms during safe-restart mode. The charging current (see symbol 'Irestart-prot' in Chapter "Characteristics") from the start-up circuit during the safe-restart mode is lower than the normal start-up current (see symbol 'Istart-high' in Chapter "Characteristics") in order to implement a low "hiccup" duty cycle. This helps insure devices on the output secondary winding do not get destroyed during output short circuit, violating safety conditions.
The start-up current source also plays a key role in implementation of burst mode stand-by (see symbol 'Irestart-stby' in Chapter "Characteristics"), which will be explained later.



(1) Start-up current charges capacitor V_{aux}.
(2) Charging of capacitor V_{aux} is taken-over by the auxiliary winding.

Fig.4 Normal start-up waveforms.



(1) Start-up current source charges capacitor V_{aux}.

Fig.5 Safe-start mode waveforms.

Reference

All reference voltages are derived from a temperature compensated, on-chip, band gap. The band gap reference voltage is also used, together with an external resistor connected at pin Iref, to generate accurate, temperature independent, bias currents in the chip:

$$I_{REF} = \frac{V_{REF}}{R_{REF}} \text{ [A]}$$

The frequency of the controller is also set by the reference resistor Rref (also see Section “Oscillator”).

Sample and hold

GreenChip™ ICs employ voltage mode feedback for regulating the output voltage. In primary feedback mode, a novel sample and hold circuit is used. The sample and hold circuit works by sampling the current into pin Dem, which is related to the output voltage via Rdem, during the time that the secondary current is flowing:

$a \times V_{out} = I_{ref} \times R_{dem} + V_{dem+}$ where:

V_{dem+} is specified in chapter “Characteristics”

a = a constant determined by turn ratio of the transformer.

This sampled current information is stored on the external capacitor connected to pin Vctrl. The pulse width modulator uses this voltage information to set the duty cycle of operation for the power MOSFET. In secondary feedback, the feedback voltage is provided by an opto-coupler.

Pulse width modulator

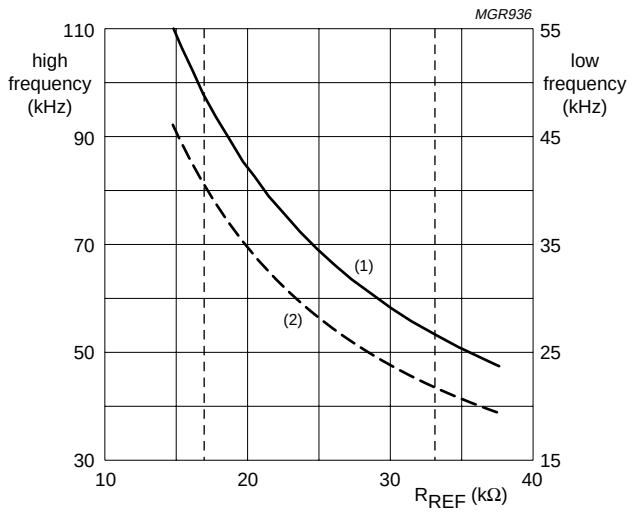
The pulse width modulator, which is made up of an inverting error amplifier and a comparator (see Fig.2), drives the power MOSFET with a duty cycle which is inversely proportional to the voltage on pin Vctrl.
In primary feedback mode, this is the voltage on the sample and hold capacitor and in secondary feedback mode, this voltage is provided by an opto-coupler. A signal from the oscillator sets a latch that turns on the power MOSFET. The latch is reset by the signal from the pulse width modulator or by the duty cycle limiting circuit.
The latching PWM mode of operation prevents multiple switching of the power switch. The maximum duty cycle is set internally at 80%.

Figure 7 shows the normal switching operation of the IC.

Oscillator

The oscillator is used to set the switching duty cycle by comparing the oscillator ramp to the output of the error amplifier in the pulse width modulator circuit.The oscillator is fully integrated and works by charging and discharging an internal capacitor between two voltage levels to create a sawtooth waveform with a rising edge which is 80% of the oscillator cycle. This ratio is used to set a maximum switching duty cycle of 80% for the IC. The oscillator is internally trimmed to 5% accuracy. The oscillator frequency can be adjusted between 50 to 100 kHz (see symbol $f_{osc\text{-}h\text{-}range}$ in Chapter “Characteristics”) by changing the external reference resistor (see symbol Rref in Chapter “Characteristics”) that sets the chip bias currents. This gives additional flexibility to the power supply designer in the choice of his system components.The frequency is correlated with the value of the reference resistor Rref (see Fig.6).

In Chapter “Characteristics” $f_{osc\text{-}typical}$, $f_{osc\text{-}l}$ and $f_{osc\text{-}h}$ and the Rref operating resistor range are specified.



(1) High frequency mode.
(2) Low frequency mode.

Fig.6 Frequency as function of the R_{REF} value.

Multi frequency control

The oscillator is also capable of working at a lower frequency (see $f_{osc\text{-}l}$ in Chapter “Characteristics”). A ratio of 1 : 2.5 is maintained between high and low frequency of the oscillator. Low frequency operation is invoked if the power supply is working at or below one ninth of its peak power. By working at a lower frequency, the switching losses in the power supply are reduced. A novel scheme is used to ensure that the transfer of high to low frequency and vice versa has no effect on the regulation of the output voltage.

Gate driver

The gate driver has a totem-pole output stage that has current sourcing capability of 120 mA and a current sink capability of 550 mA. This is to enable fast turn on and turn off of the power device for efficient operation.

A lower driver source current has been chosen in order to limit the $\Delta V/\Delta t$ at switch-on. This is advantageous for EMI (ElectroMagnetic Interference) and reduces the current spike across Rsense.

Demagnetization protection

This feature guarantees discontinuous conduction mode operation for the power supply which simplifies the design of feedback control and gives faster transient response.

Demagnetization protection is an additional protection feature that protects against saturation of the transformer/inductor. Demagnetization protection also protects the power supply components against excessive stresses at start-up, when all energy storage components are completely discharged. The converter is cycle by cycle protected during shorted output system fault condition due to the demagnetization protection. The value of the demagnetization resistor (R_{dem}) can be calculated with the formula given in Section “Sample and hold”.

Negative clamp

The negative clamp circuit does not let the voltage on pin Dem go below −0.4 V, when the auxiliary winding voltage goes negative during the time that the power device is turned on, to ensure correct operation of the IC.

Over voltage protection

An Over Voltage Protection (OVP) mode has been implemented in the GreenChip™ series. This circuit works by sensing the Vaux voltage. If the output voltage exceeds the preset voltage limit, the OVP circuit turns off the power MOSFET. With no switching of the power device, the Vaux capacitor is not re-supplied and discharges to UVLO level and the system goes into the low dissipation safe-restart mode described earlier. The system recovers from the safe-restart mode only if the OVP condition is removed.

Over current protection

Cycle by cycle Over Current Protection (OCP) is provided by sensing the voltage on an external resistor which is connected to the source of the power MOSFET.
The voltage on the current sense resistor, which reflects the amplitude of the primary current, is compared internally with a reference voltage using a high speed comparator. This threshold voltage is specified as $V_{th(Imax)}$ in the chapter “Characteristics”. The maximum primary (protection) current is therefore: $I_{prot} = \frac{V_{th(Imax)}}{R_{sense}}$ [A]

If the power device current exceeds the current limit, the comparator trips and turns off the power device.
The power device is typically turned off in 210 ns (see t_D in Chapter “Characteristics”).

The availability of the current sense resistor off-chip for programming the OCP trip level increases design flexibility for the power supply designer. An off-chip current sense resistor also reduces the risk of an OCP condition being sensed incorrectly. At power MOSFET turn-on the $\Delta V/\Delta t$ limiters capacitance discharge current does not have to flow through the sense resistor, because this capacitor can be connected between drain and source of the power MOSFET directly.

The Leading Edge Blanking (LEB) circuit works together with the OCP circuit and inhibits the operation of the OCP comparator for a short duration (see t_{LEB} in Chapter “Characteristics”) when the power device is turned on. This ensures that the power device is not turned off prematurely due to false sensing of an OCP condition because of current spikes caused by discharge of primary-side snubber and parasitic capacitances.
LEB time is not fixed and it tracks the oscillator frequency.

Over temperature protection

Protection against excessive temperature is provided by an analog temperature sensing circuit that turns off the power device when the temperature exceeds typically 140 °C.

On/off mode

The expensive mains switch can be replaced by an in-expensive functional switch by using the on/off mode. Figure 13 shows a flyback converter configured to use the on/off mode. Depending upon the position of switch S1, either voltage close to ground or a voltage of greater than typical 2.5 V exists on pin OOB.

The difference between these voltages is detected internally by the IC. The IC goes into the off-mode if the voltage is low, where it consumes a current of typical 350 μA (see Iin-off in Chapter “Characteristics”). If the voltage on pin OOB is typically 2.5 V (see Von/off in Chapter “Characteristics”), the IC goes through the start-up sequence and commences normal operation.

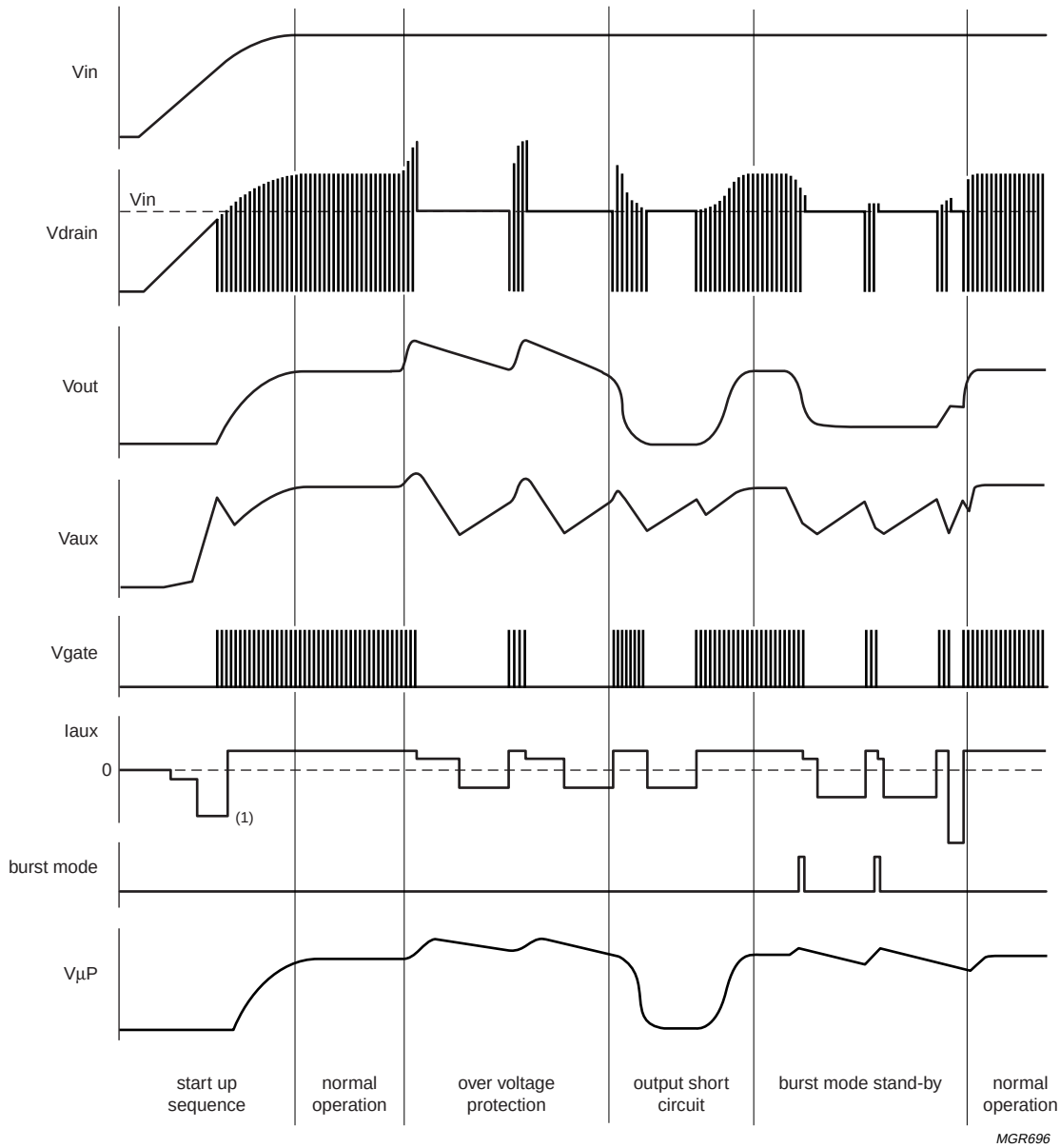
In Fig.14 a Mains Under Voltage Lock Out (MUVLO) function has been created using 3 resistors. Assuming that R3 is chosen very high ohmic, the GreenChip™ starts operating if: $V_{MAINS} \approx \frac{R1}{R2} \times V_{OOB} \; (R1 \gg R2)$

In this way it is assured that the power supply only starts working above a Vmains of e.g. 80 V. The bleeder current through R1 should be low (e.g. 30 μA at 300 V).

Burst mode stand-by

Pin OOB is also used to implement the burst mode stand-by. In burst mode stand-by, the power supply goes into a special low dissipation state where it typically consumes less than 2 W of power. Figure 14 shows a flyback converter using the burst mode stand-by feature. The system enters burst mode when the microcontroller closes switches S2 and S3 on the secondary side. Switch S2 shorts the output capacitor to the voltage level of the microcontroller capacitor. The output secondary winding now supplies the microcontroller capacitor. When the voltage on the microcontroller capacitor exceeds the zener voltage (V_z) the opto-coupler is activated which sends a signal to pin OOB. In response to this signal, the IC stops switching and goes into a “hiccup” mode.

Figure 7 shows the burst-mode operation graphically. The hiccup mode during burst mode operation differs from the hiccup in safe-restart mode during system fault. For safe restart mode, the power has to be reduced. For burst mode, sufficient power to supply the microcontroller has to be delivered. To prevent transformer rattle, the transformer peak current is reduced by a factor of 3. Burst mode stand-by operation continues till the microcontroller opens switches S2 and S3. The system then goes through the start-up sequence and commences normal switching behaviour.



(1) All negative currents are currents out the chip.

Fig.7 Typical waveforms.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); unless noted all voltages are measured with respect to pin GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{I(max)}$	maximum DC input voltage		–	600	V
		during inductive turn-off; note 1	–	720	V
I_D	supply current		–	7	A
V_{OOB}	mode detect input voltage		–0.3	+14	V
I_{OOB}	mode detect input current		–	+2	mA
I_{demag}	demagnetization input current		–	±1	mA
V_{ctrl}	feedback input voltage		–0.3	+5	V
V_{Isense}	current sense input voltage		–0.3	+5	V
I_{ref}	reference input current		–	–1	mA
V_{aux}	auxiliary supply voltage		–0.3	+18	V
T_j	operating junction temperature		–10	+140	°C
T_{stg}	storage temperature		–40	+150	°C
V_{es}	electrostatic handling voltage	class 2			
		human body model; note 3	–	2500	V
		machine model; note 4	–	250	V

Notes

1. Repetitive clamped inductive turn-off energy <15 mJ.
2. Single pulse avalanche energy at T_j < 25 °C: 570 mJ.
3. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
4. Equivalent to discharging a 200 pF capacitor through a 0.75 mH coil.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
IC controller			
$R_{th(j-a)}$	thermal resistance from junction to ambient	70	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	31	K/W
Power FET			
$R_{th(j-a)}$	thermal resistance from junction to ambient	37	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	0.85	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611 part E”*.

CHARACTERISTICS

T_j = –10 to +110 °C; V_{in} = 300 V; V_{aux} = 8.6 to 13 V; R_{Iref} = 24.9 kΩ ±0.1%; all currents into the chip are positive and all currents out of the chip are negative; all voltages are measured with respect to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage and current on pin 9						
V_{dlow}	minimum start drain voltage		100	–	–	V
I_{in}	input current	normal operation	20	60	100	µA
$I_{in(off)}$	off mode current	V_{OOB} < 1.95 V	150	350	550	µA
Start-up current source and Vaux management on pin 2						
V_{start}	start-up voltage		10.4	11	11.6	V
V_{uvlo}	under voltage lockout		7.4	8.05	8.6	V
V_{hys}	operation voltage hysteresis	V_{start}-V_{uvlo}	2.60	2.95	3.30	V
$I_{start(low)}$	start-up current	0 V < V_{aux} < 0.5 V	–270	–230	–190	µA
$I_{start(high)}$	start-up current	0.5 V < V_{aux} < V_{start}	–5.0	–3.0	–1.0	mA
I_{aux}	IC supply current	in high frequency mode	7.0	7.7	8.5	mA
$I_{restart(prot)}$	restart current	in protection mode	–600	–530	–460	µA
$I_{restart(stdby)}$	restart current	in stand-by mode	–2.5	–2.1	–1.7	mA
V_{clamp}	clamp voltage level	I_{aux} = 5 mA (non switching)	15	–	18	V
Reference input on pin 3						
V_{ref}	reference voltage	capacitor pin Iref = 50 nF	2.37	2.47	2.57	V
R_{ref}	operating resistor range		16.9	24.9	33.2	kΩ
Oscillator						
f_{osc-l}	low frequency	low power mode; C_{IREF} = 50 nF	27.5	29	30.5	kHz
f_{osc-h}	high frequency	normal mode; C_{IREF} = 50 nF	66	70	74	kHz
δ_{max}	maximum duty cycle	f = f_{osc-h}	78	80	82	%
f_{ratio}	ratio f_{osc-h}/f_{osc-l}		2.30	2.45	2.60	
$f_{osc-h-range}$	range of f_{osc-h}	with changing R_{IREF}	50	70	100	kHz
Demagnetization input on pin 6						
$V_{th(comp)}$	demag comparator threshold	V_{dem} decreasing	50	65	80	mV
t_{PD}	propagation delay to output buffer		300	500	700	ns
I_{bias}	input bias current	V_{dem} = 65 mV	–0.50[1]	–	–0.10[1]	µA
$V_{clamp(neg)}$	negative clamp level	I_{dem} = –500 µA	–0.45	–0.35	0	V
$V_{clamp(pos)}$	positive clamp level	I_{dem} = 100µA	2.3	2.6	2.9	V
Sample and hold input on pin 6						
I_{dem}	normal control current	Iref = 100 µA	90	100	110	µA
$I_{th(sh)}$	sample threshold current	% of Idem	78	83	88	%
t_{PD}	propagation delay of current comparator	δVdemag/δt positive	170	450	730	ns
		δVdemag/δt negative	20	90	160	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Over voltage protection on pin 2						
V_{OVP}	absolute maximum OVP level	fixed maximum level	14.0	14.7	15.5	V
$t_{d(OVP)}$	OVP delay time		350	550	800	ns
Isense and low power on pin 1						
t_{LEB}	leading edge blanking time	$R_{ref} = 0.7 \times R_{ref(nom)}$	180	260	340	ns
		$R_{ref} = R_{ref(nom)}$	240	340	440	ns
		$R_{ref} = 1.3 \times R_{ref(nom)}$	415	470	560	ns
$V_{th(Imax)}$	maximum current limit voltage		0.46	0.49	0.53	V
t_d	delay to MOSFET off	time to MOSFET off at dV/dt = 200 mV/µs; Cgs = 500 pF	150	210	270	ns
$V_{th(lopower)}$	threshold voltage	for switch over to low power	155	165	175	mV
Control						
dδ/dV	gain	f_{osc-h}	–95	–85	–75	%/V
		f_{osc-l}	–60	–50	–40	%/V
$V_{CTRL(min)}$	minimum control voltage on pin 4		2.00	2.15	2.30	V
$V_{CTRL(max)}$	maximum control voltage on pin 4		2.90	3.05	3.20	V
$I_{CTRL(leak)}$	leakage current in/out on pin 4	note 1	–1	–	+1	µA
Over temperature protection						
T_{trip}	temperature limit		130	140	155	°C
On/off/burst mode selection input on pin 7						
$V_{on/off}$	on/off trip level		2.3	2.5	2.8	V
V_{burst}	burst mode trip level	active	6.5	–	7.5	V
		inactive	–	–	5.5	V
I_{OOB}	output current on pin OOB	V_{OOB} > 400 mV; note 1	–5	–	-0.1	µA
Power MOSFET 7N60E; note 2						
$V_{DS(break)}$	drain-to-source breakdown voltage	T_j = 25 °C; Vgs = 0 V; Id = 0.25 mA	600	–	–	V
$R_{DS(on)}$	drain-to-source on-state resistance	T_j = 25 °C; Vgs = 10 V; Vaux = 10 V; Id = 7A	–	1.0	1.2	Ω

Notes

1. Min. and max. values are guaranteed by design.
2. The power MOSFET outputs of these devices are similar to the Philips Semiconductor type PHP7N60. These devices feature an excellent combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

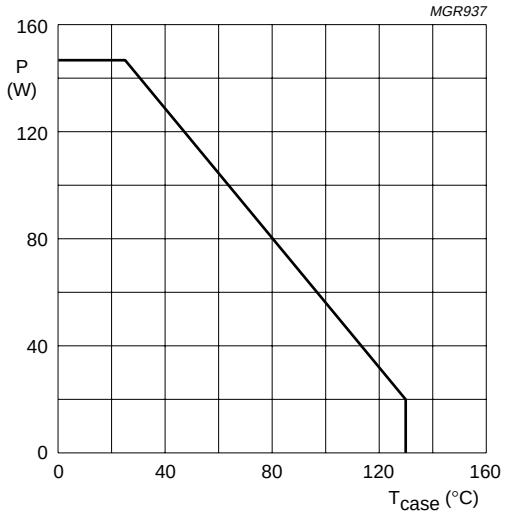


Fig.8 Normalised power derating.

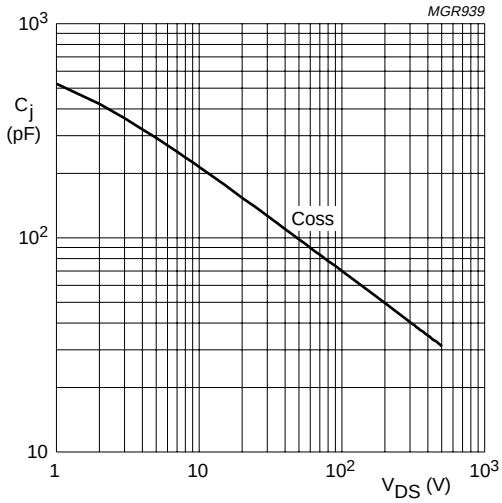
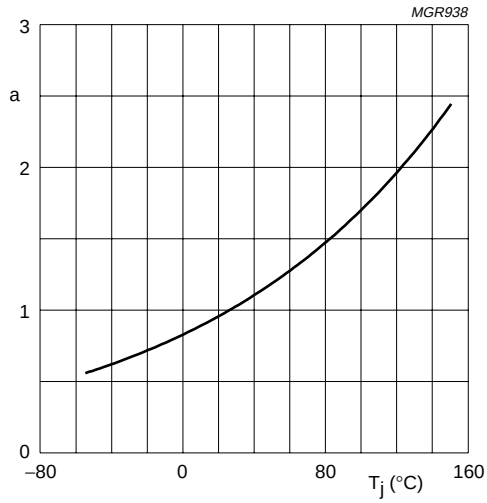


Fig.9 Junction capacitance.



$a = R_{DS(on)} / R_{DS(on)}$ at 25 °C.
I_D = 6.2 A; V_{aux} > 10 V.

Fig.10 Normalised drain-to-source on-state resistance.

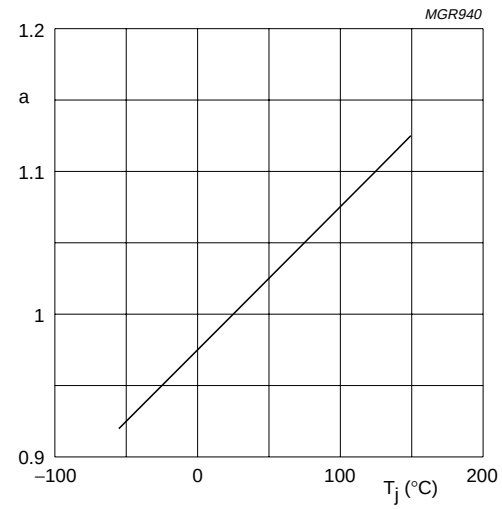
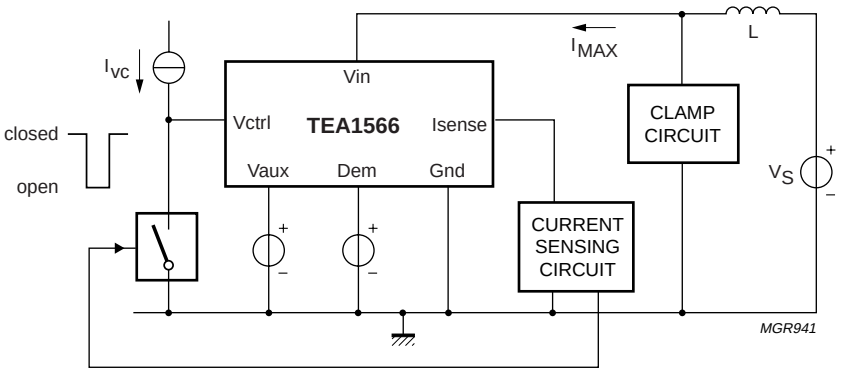


Fig.11 Normalised drain-to-source breakdown voltage.



V_S = 50 V; I_{MAX} = 7 A
V_{dem} = 0.5 V; V_{aux} = 11 V
I_{VC} = 6 mA; V_{CLAMP} = 720 V
L = 25 mH

Fig.12 Clamped inductive test circuit.

APPLICATION INFORMATION

A converter using the GreenChip™ is usually a flyback or a Buck converter that is made up of the EMI filter, full bridge rectifier, filter capacitor, transformer, output stage(s), and some snubber circuitry.

Depending upon the type of feedback used, either an auxiliary winding (primary regulation) or an opto-coupler (secondary regulation) is used. GreenChip™, due to its high level of integration uses very few external components. A sense resistor converts the primary current into a voltage on pin Isense. The IC uses this information for setting the peak current in the converter.

A capacitor supplied by an auxiliary winding buffers the internal supply of the IC and is connected on pin Vaux.

The auxiliary winding is also used for primary mode output voltage regulation. A resistor connected on pin Iref sets the reference currents in the IC. A small capacitor (0.2 to 2 nF) connected on pin Vctrl is used by the internal sample and hold circuit for regulation in primary feedback scheme. The same pin is also used for secondary sensing and serves as the input for the signal from the opto-coupler.

Pin Gnd is the ground connection pin.

The primary side auxiliary winding is connected via a resistor to pin Dem. Besides being used for demagnetization protection, pin Dem is also used for primary side regulation.

Pin OBB is a multi use pin and depending upon connection can be used for implementation of the on/off/burst mode functions.

Pin 8 is not connected and serves as a high voltage spacer pin.

Pin Vin is the connection for the drain of the internal power MOSFET and is a high voltage pin. The internal start-up current source also uses this pin as a supply for charging up the Vaux capacitor during start-up and safe-restart modes.

GreenChip™ is a versatile IC that can be used in flyback and Buck converter topologies and can be configured to work in different modes. The application diagrams on the next pages give some examples.

For additional information also see:

- ***Application note AN98011: "200 W SMPS with TEA1504"***
- ***Application note AN98058: "75 W SMPS with TEA1566"***.

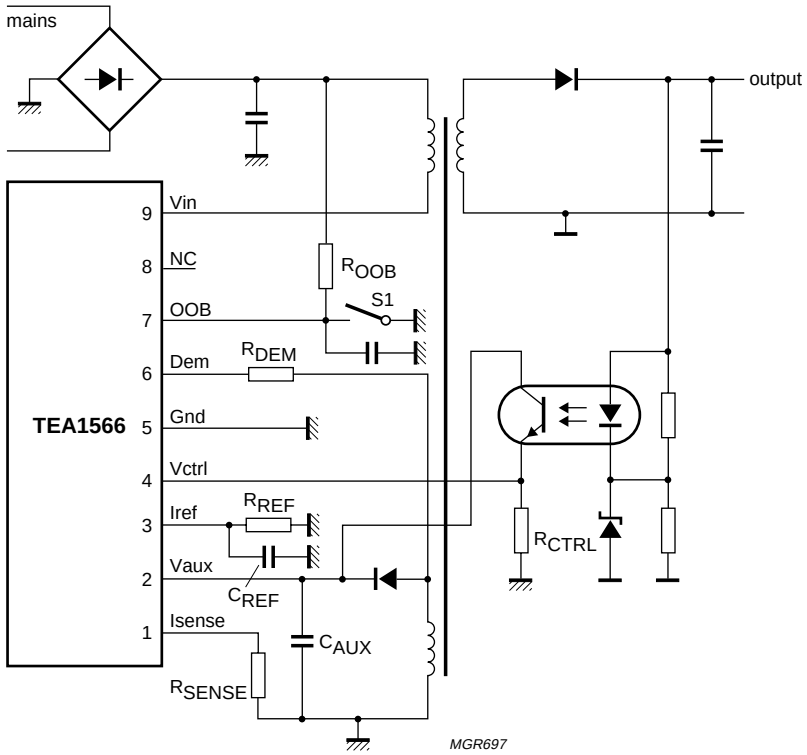


Fig.13 Typical flyback configuration with secondary sensing and on/off feature.

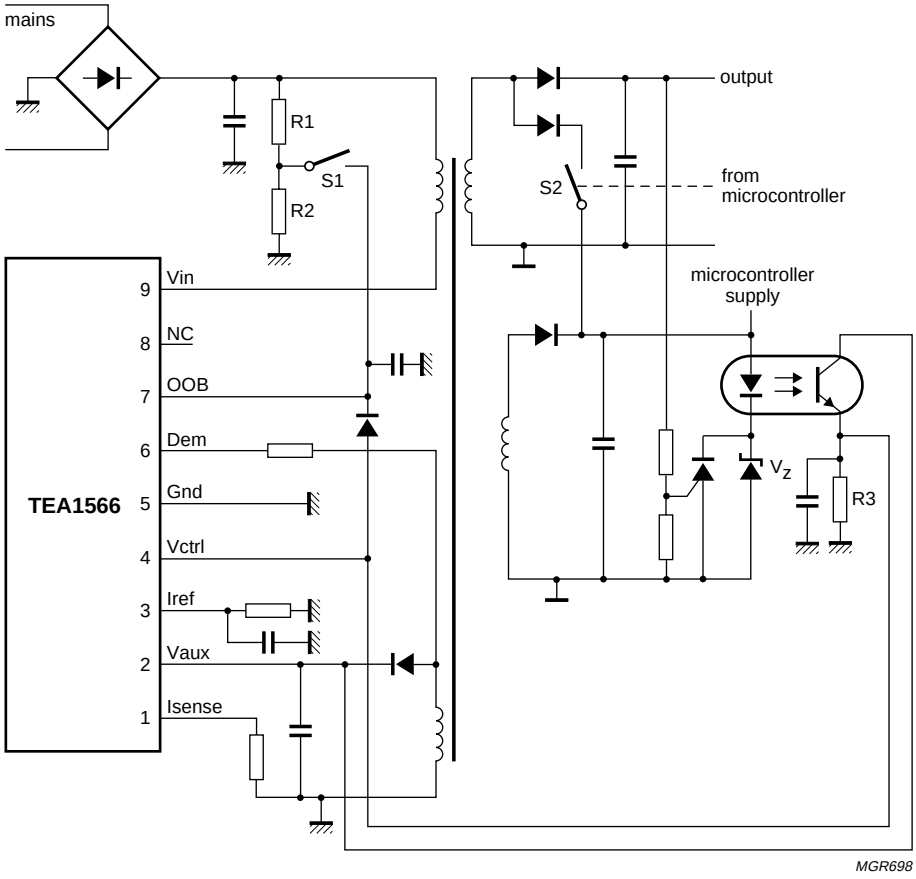


Fig.14 Flyback configuration using the burst mode stand-by, MUVLO and on/off features.

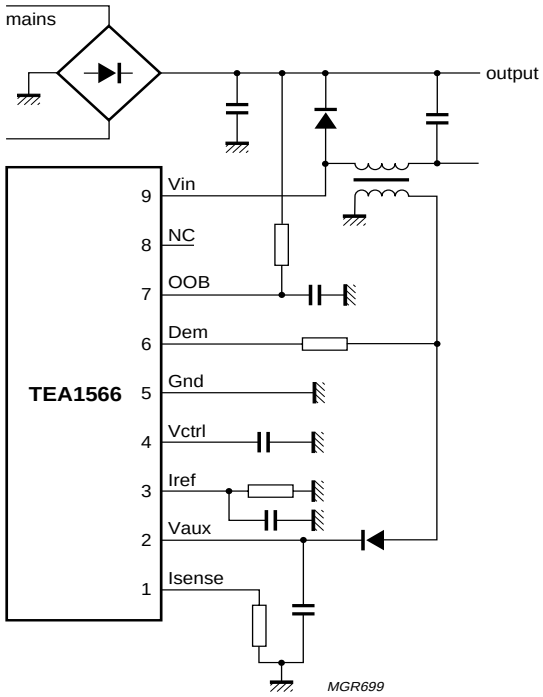


Fig.15 Typical Buck configuration with primary sensing.

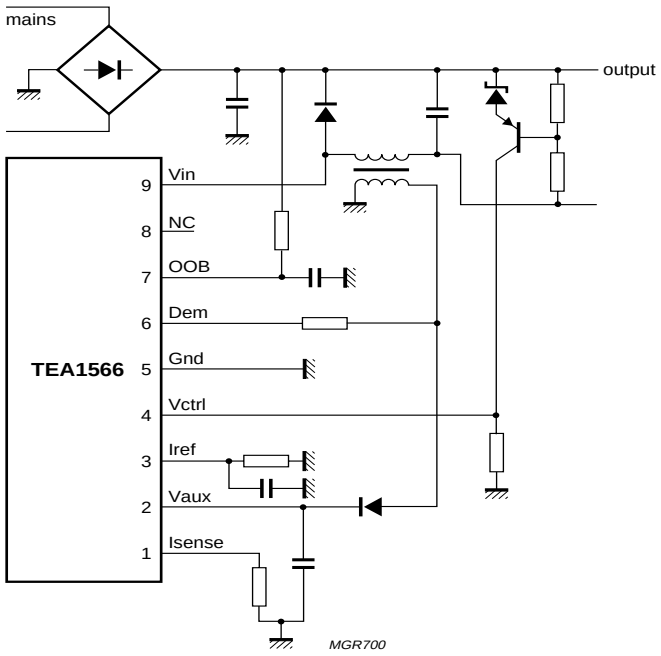
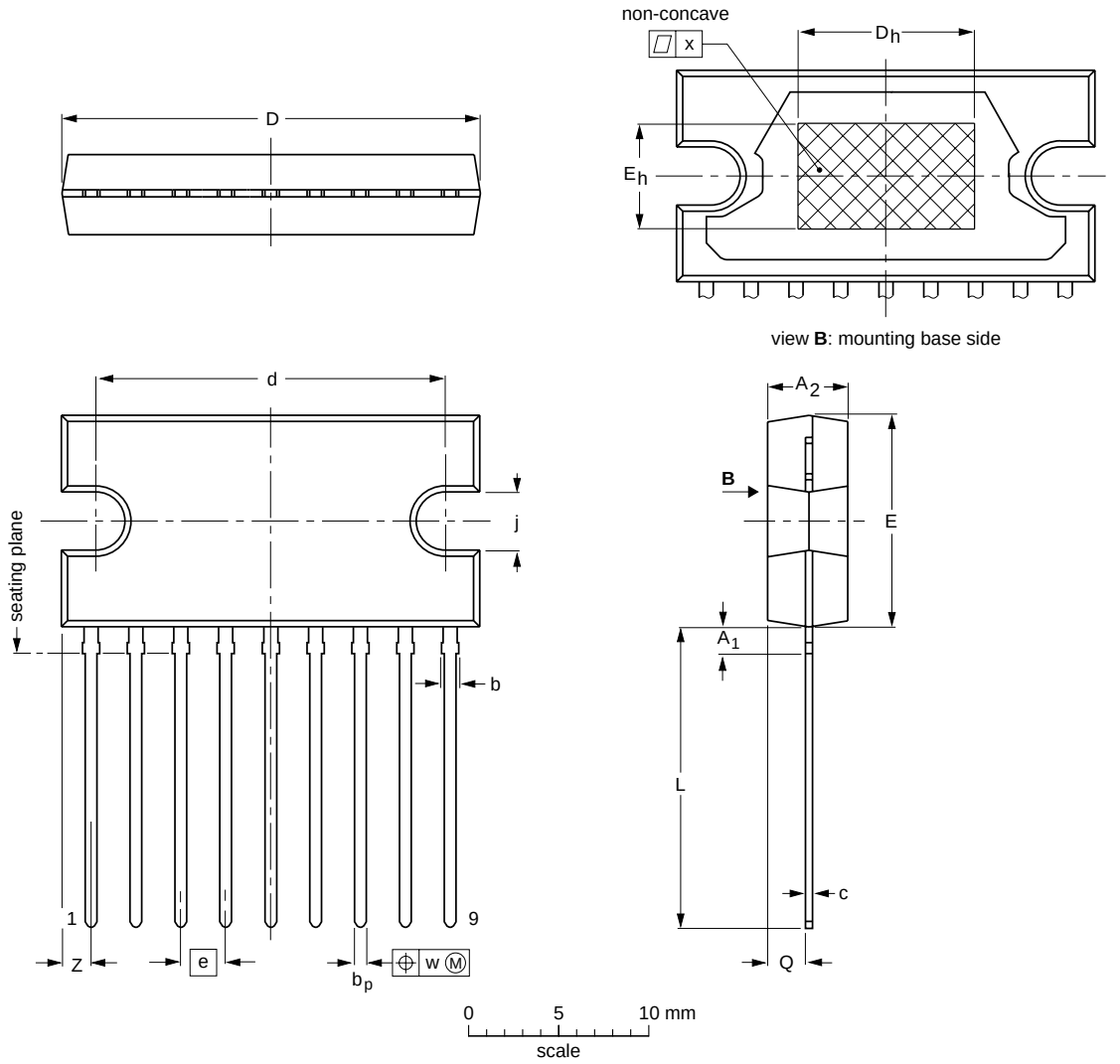


Fig.16 Typical Buck configuration with secondary sensing.

PACKAGE OUTLINES

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

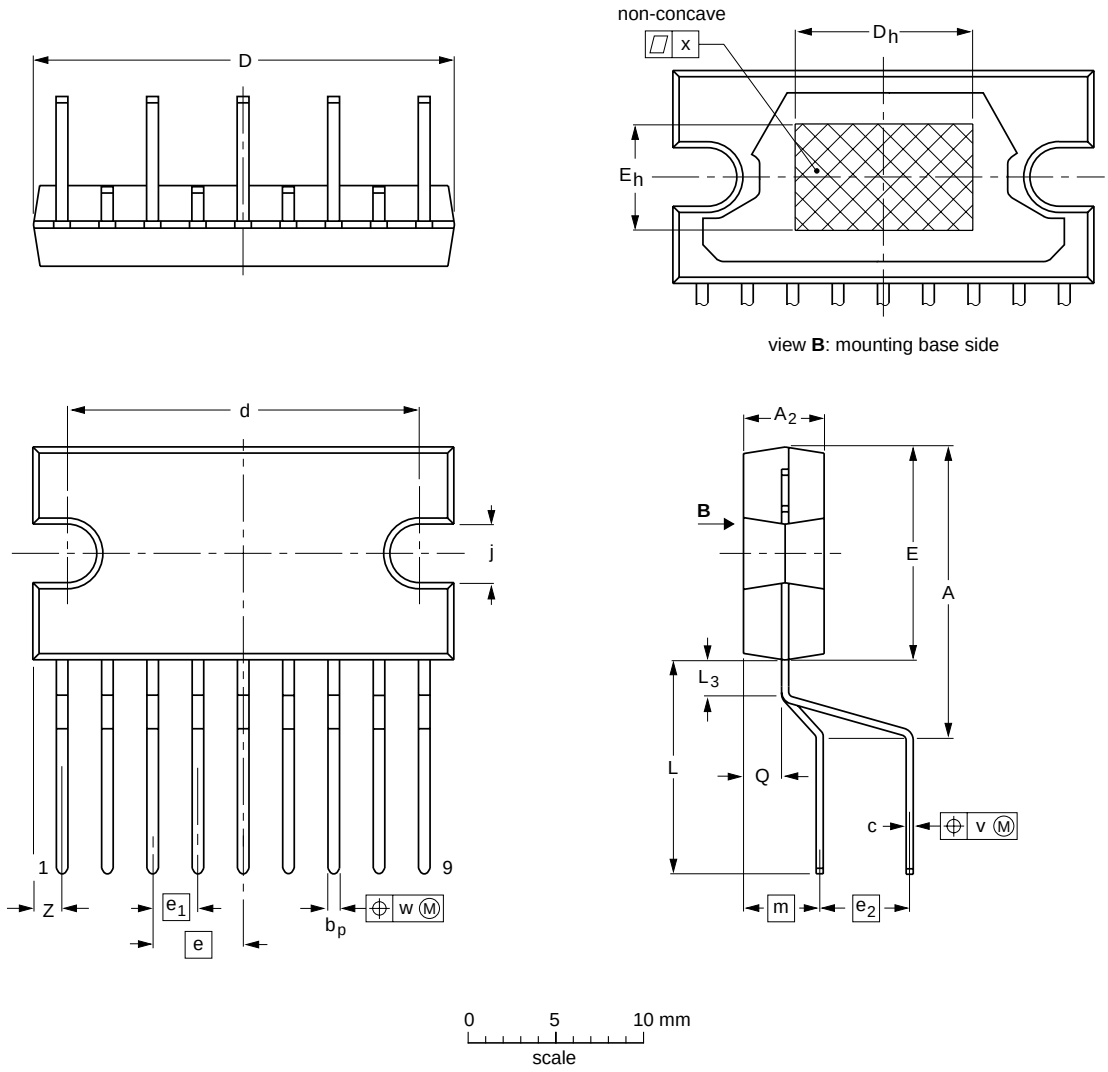
UNIT	A_1 max.	A_2	b max.	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	Q	w	x	$Z^{(1)}$
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~92-11-17~~ 95-03-11

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm) **SOT157-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	5.08	2.54	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT157-2						~~95-03-11~~ 97-12-16

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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